

What is claimed is:

1 1. A method comprising:
2 determining utilization values for a plurality of
3 processors having power utilization dependencies; and
4 identifying a target frequency for the plurality of
5 processors based on the utilization values.

1 2. The method of claim 1, further comprising
2 transitioning a processor package to the target frequency,
3 the processor package including the plurality of
4 processors.

1 3. The method of claim 1, further comprising
2 obtaining parameter information for the plurality of
3 processors.

1 4. The method of claim 3, further comprising
2 determining the utilization values using the parameter
3 information.

1 5. The method of claim 1, wherein the utilization
2 values comprise an up/down decision for each of the
3 plurality of processors.

1 6. The method of claim 2, wherein identifying the
2 target frequency comprises identifying a frequency

3 operating point closest to a maximum operating frequency of
4 the processor package multiplied by a maximum utilization
5 of one of the plurality of processors having a highest
6 value for the maximum utilization.

1 7. The method of claim 2, further comprising
2 transitioning the processor package to a higher frequency
3 if one of the utilization values is an up decision.

1 8. The method of claim 2, further comprising
2 transitioning the processor package to a lower frequency if
3 all of the utilization values are a down decision.

1 9. The method of claim 1, wherein the plurality of
2 processors comprise a plurality of logical processors.

1 10. The method of claim 1, wherein the plurality of
2 processors comprise at least one multicore processor.

1 11. A method comprising:
2 determining utilization decisions for logical
3 processors of a physical processor using parameter
4 information; and
5 calculating a target frequency for the physical
6 processor based on the utilization decisions.

1 12. The method of claim 11, further comprising
2 transitioning the physical processor to the target
3 frequency.

1 13. The method of claim 11, further comprising
2 transitioning the physical processor to a higher frequency
3 if any of the logical processors has an up utilization
4 decision.

1 14. The method of claim 13, wherein the higher
2 frequency is based on a highest utilization processor of
3 the logical processors.

1 15. The method of claim 11, further comprising
2 transitioning the physical processor to a lower frequency
3 if all of the logical processors have a down utilization
4 decision.

1 16. The method of claim 15, wherein the lower
2 frequency is based on a highest utilization processor of
3 the logical processors.

1 17. The method of claim 12, wherein transitioning the
2 physical processor comprises transitioning to a higher
3 frequency if any of the logical processors needs additional
4 compute power.

1 18. The method of claim 11, wherein calculating the
2 target frequency is based on desired power and performance
3 characteristics.

1 19. An article comprising a machine-readable storage
2 medium containing instructions that if executed enable a
3 system to:

4 determine utilization values for a plurality of
5 processors having power utilization dependencies; and
6 identify a target frequency for the plurality of
7 processors based on the utilization values.

1 20. The article of claim 19, further comprising
2 instructions that if executed enable the system to
3 transition a processor package to the target frequency, the
4 processor package including the plurality of processors.

1 21. The article of claim 20, further comprising
2 instructions that if executed enable the system to identify
3 a frequency operating point closest to a maximum operating
4 frequency of the processor package multiplied by a maximum
5 utilization of one of the plurality of processors having a
6 highest value for the maximum utilization.

1 22. The article of claim 20, further comprising
2 instructions that if executed enable the system to
3 transition the processor package to a higher frequency if
4 any of the plurality of processors needs additional compute
5 power.

1 23. The article of claim 20, further comprising
2 instructions that if executed enable the system to
3 transition the processor package to a lower frequency if
4 any of the plurality of processors needs less power.

1 24. A system comprising:
2 a plurality of processors; and
3 a dynamic random access memory containing instructions
4 that if executed enable the system to determine utilization
5 values for the plurality of processors and to identify a
6 target frequency for the plurality of processors based on
7 the utilization values.

1 25. The system of claim 24, wherein the plurality of
2 processors comprises a plurality of logical processors
3 within a processor package.

1 26. The system of claim 25, further comprising
2 instructions that if executed enable the system to identify
3 a frequency operating point closest to a maximum operating
4 frequency of the processor package multiplied by a maximum

5 utilization of one of the plurality of logical processors
6 having a highest value for the maximum utilization.

1 27. The system of claim 25, further comprising
2 instructions that if executed enable the system to
3 transition the logical processor package to a higher
4 frequency if any of the plurality of logical processors
5 needs additional compute power.